Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-4 (canceled)

Claim 5 (currently amended): A semiconductor device, ~~comprising: combining and disposing means for~~ which is formed by combining and disposing pre-registered functional blocks, and ~~wiring means for~~ determining a wiring pattern in accordance with a given logic circuit specification, ~~wherein~~ at least one of the functional blocks ~~has~~ comprising:

a logic circuit, and,

a diode, ~~the diode~~ which is composed of a first conduction type diffusion layer and a second conduction type well connected to a power source, ~~and~~

wherein the diode is connected to a potential-clamped input terminal of the at least one of the functional blocks.

Claim 6 (previously presented): The semiconductor device as claimed in Claim 5, wherein the logic circuit is a memory.

Claim 7 (previously presented): A method of designing a semiconductor device, comprising the steps of:

combining and disposing pre-registered functional blocks, and

determining a wiring pattern in accordance with a given logic circuit specification,

wherein at least one of the functional blocks has a logic circuit and a diode,

the diode is composed of a first conduction type diffusion layer and a second conduction type well connected to a power source, and

the diode is connected to a potential-clamped input terminal of the at least one of the functional blocks.

Claim 8 (previously presented): A computer-readable recording medium, on which the method of designing a semiconductor device, as claimed in Claim 7, is stored as a program to be executed by a computer.

Claim 9 (previously presented): A design support apparatus for a semiconductor device, comprising:

combining and disposing means for combining and disposing pre-registered functional blocks, and

wiring means for determining a wiring pattern in accordance with a given logic circuit specification,

wherein at least one of the functional blocks has a logic circuit and a diode, and

wherein the diode is composed of a first conduction type diffusion layer and a second conduction type well connected to a potential-clamped input terminal of the at least one of the functional blocks.

Claim 10 (currently amended): A semiconductor device, ~~comprising: combining and disposing means for combining~~ which is formed by combing and disposing pre-registered functional blocks, and

~~wiring means for~~ determining a wiring pattern in accordance with a given logic circuit specification,

wherein at least one of the functional blocks has a logic circuit and a diode which is at least connected to an input pin where results of an antenna ratio exceed an allowed antenna ratio,

the diode is composed of a first conduction type diffusion layer and a second conduction type well connected to a power source, and

the diode is connected to a potential-clamped input terminal of the at least one of the functional blocks.

Claim 11 (previously presented): The semiconductor device as claimed in Claim 10, wherein the logic circuit is a memory.

Claim 12 (previously presented): A method of designing a semiconductor device, comprising the steps of:

combining and disposing pre-registered functional blocks, and

determining a wiring pattern in accordance with a given logic circuit specification,

wherein at least one of the functional blocks has a logic circuit and a diode which is at least connected to an input pin where results of an antenna ratio exceed an allowed antenna ratio,

wherein the diode is composed of a first conduction type diffusion layer and a second conduction type well connected to a power source, and

the diode is connected to a potential-clamped input terminal of the at least one of the functional blocks.

Claim 13 (previously presented): A computer-readable recording medium, on which the method of designing a semiconductor device, as claimed in Claim 12, is stored as a program to be executed by a computer.

Claim 14 (currently amended): A design support apparatus for a semiconductor device[[,]] <u>comprising:</u>

combining and disposing means for combining and disposing pre-registered functional blocks, and

wiring means for determining a wiring pattern in accordance with a given logic circuit specification,

wherein at least one of the functional blocks has a logic circuit and a diode which is at least connected to an input pin where results of an antenna ratio exceed an allowed antenna ratio, and

wherein the diode is composed of a first conduction type diffusion layer and a second conduction type well connected to a potential-clamped input terminal of the at least one of the functional blocks.

Claim 15 (previously presented): The semiconductor device as claimed in Claim 5, wherein the diode is connected to a port between an output of the logic circuit and the input terminal of the functional block.

Claim 16 (new): A semiconductor device comprising at least one functional block having a logic circuit and a diode composed of a first conduction type diffusion layer and a second conduction type well connected to a power source, wherein the diode is connected to a potential-clamped input terminal of the at least one functional block.

Claim 17 (new): The semiconductor device as claimed in Claim 16, wherein the logic circuit is a memory.

Claim 18 (new): The semiconductor device as claimed in Claim 16, wherein the diode is connected to a port between an output of the logic circuit and the input terminal of the functional block.

Claim 19 (new): A semiconductor device comprising at least one functional block having a logic circuit and a diode which is at least connected to an input pin where results of an antenna ratio exceed an allowed antenna ratio, wherein the diode is composed of a first conduction type diffusion layer and a second conduction type well connected to a power source and wherein the diode is connected to a potential-clamped input terminal of the at least one of the functional blocks.

Claim 20 (new): The semiconductor device as claimed in Claim 19, wherein the logic circuit is a memory.